Application No.: 09/588,617 Docket No.: 21806-00083-US

REMARKS

Claims 1-32 remain pending in this application. Claims 1, 30, and 32 are independent. Claims 1, 30, and 32 have been amended, and no claims have been canceled or added by this amendment.

Withdrawal of the rejection of claims 1-29 under 35 U.S.C. §112, first paragraph, for lack of written description, is requested. Applicants submit that a person with skill in the art would appreciate and understand the concept and context of "interconnect wiring...sufficient for both testing and end use operation of said semiconductor devices", as recited in original claim 1, particularly in light of the Specification at, for example, page 16, lines 21-24 and at page 19, lines 7-24.

However, to expedite prosecution of this application and passage to issue, independent claim 1 has been amended to recite "packaging" instead of "end use operation", thus rendering the §112 (¶1) rejection moot.

Anticipation Rejection

Withdrawal of the rejection of claims 1-32 under 35 U.S.C. §102(b) as being anticipated by Rostoker et al. (US 5,594,626).

Applicant notes that anticipation requires the disclosure, in a prior art reference, of each and every limitation as set forth in the claims.[1] There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. §102.[2] To properly anticipate a claim, the reference must teach every element of the claim.[3] "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference".[4] "The identical invention must be shown in

[1] *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985).
[2] *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991).
[3] *See* MPEP § 2131.
[4] *Verdegaal Bros. v. Union Oil Co. of Calif.*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

PAGE 8/14 * RCVD AT 1/9/2004 7:44:31 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:202 293 6229 * DURATION (mm-ss):03-54

as complete detail as is contained in the ...claim."[5] In determining anticipation, no claim limitation may be ignored.[6]

Deficiencies of Rostoker et al.

The applied art does not disclose a method for manufacturing and testing semiconductor components, which includes, among other features, "...providing a device carrier...having interconnect wiring therein sufficient for both operational testing and packaging of said semiconductor devices...testing said devices via said wiring; and dividing said carrier into a plurality of components wherein each said component contains at least one said semiconductor device, as recited in independent claim 1, as amended.

In addition, the applied art does not disclose a semiconductor structure which includes, among other features, "...a device carrier...having interconnect wiring therein sufficient for both operational testing and packaging of said semiconductor devices; wherein said semiconductor devices on said carrier are arranged to be tested and burned-in...and wherein said plurality of components are arranged so as to be suitably installed in an information handling system without separating said semiconductor devices from said device carrier", as recited in independent claim 30, as amended.

Finally, the applied art does not disclose a semiconductor structure which includes, among other features, "...a stack of flex device carriers, at least one semiconductor device mounted to each said flex carrier; and an interconnect substrate...wherein said stack of flex device carriers, said at least one semiconductor device, and said interconnect substrate are interconnected and arranged in a manner suitable for both operational testing and packaging of the semiconductor structure", as recited in independent claim 32, as amended.

Rostoker et al. is directed to a partially-molded PCB chip carrier package for non-square die shapes which have a high pin count. The non-square shape enables Rostoker et al., at least in part, to better accommodate high pin count chips, carriers, and associated leads. Applicants

[5] *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).
[6] *Pac-Tex, Inc. v. Amerace Corp.*, 14 USPQ2d 187 (Fed. Cir. 1990).

submit that Rostoker et al. does not disclose or contemplate use of interconnect wiring in a device carrier sufficient for both operational testing and packaging.

Instead, Rostoker et al. FIG. 6 illustrates an embodiment arranged with a certain perimeter-to-area ratio of a greatly elongated rectangular die-receiving area which accommodates 15% more conductive lines than a similar prior art size (square) die-receiving area. Rostoker et al. FIG. 14B illustrates a plan view of a number of greatly elongated rectangular semiconductor packages (e.g., as shown in FIG. 6) on a printed circuit mother board. Rostoker et al. FIG. 15 illustrates a plan view of a leadframe element for a package adapted to triangular die and package shapes.

None of these Figures teach or suggest the limitations in independent claims 1, 30, or 32, particularly relating to use of interconnect wiring which is sufficient for both testing and packaging of semiconductor devices, as variously claimed, and as would be understood by a person having skill in the art, in light of the Specification.

Therefore, withdrawal of the rejection and allowance of independent claims 1, 30, and 32 are requested. Further, dependent claims 2-29, variously and ultimately depend upon allowable claim 1, and dependent claim 31 depends upon allowable claim 30. Allowance of these claims is also requested.

Unpatentability Rejection

Withdrawal of the rejection of claims 13-29 under 35 U.S.C. §103(a) as being unpatentable over Rostoker et al. in view of previously cited Kaneko et al. (US 5,354,786) is requested.

At the outset, Applicant notes that, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim

PAGE 10/14 * RCVD AT 1/9/2004 7:44:31 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:202 293 6229 * DURATION (mm-ss):03-54

limitations.[7] Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.[8]

Not only does Kaneko et al. not make up for the previously identified deficiencies of Rostoker et al. at least with respect to independent claim 1, Applicants submit that proper motivation to combine the applied art in the manner suggested by the Examiner has not been established, because Kaneko et al. teaches away from at least one aspect of the claimed invention.

Rostoker et al. and Kaneko et al. do not Teach all Limitations

All the claim limitations must be taught or suggested by the prior art.[9] All words in a claim must be considered in judging the patentability of that claim against the prior art.[10]. When evaluating the scope of a claim, every limitation in the claim must be considered.[11] The evidentiary record fails to teach each limitation of the claimed invention.

Kaneko et al. does not teach or suggest, either alone or in combination, a method for manufacturing and testing semiconductor components, which includes, among other features, "...providing a device carrier...***having interconnect wiring therein sufficient for both operational testing and packaging of said semiconductor devices***...testing said devices via said wiring; and dividing said carrier into a plurality of components wherein each said component contains at least one said semiconductor device, as recited in independent claim 1, as amended.

Therefore, since the applied art does not teach or suggest all the claim limitations of independent claim 1, dependent claims 13-29 are also allowable.

---

[7] *See* MPEP §2143.
[8] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.
[9] *In re Royka* 180 USPQ 580 (CCPA 1974).
[10] *In re Wilson*, 165 USPQ 494 (CCPA 1970) and *see MPEP* § 2143.03.
[11] *In re Ochiai*. 37 USPQ2d 1127 (Fed. Cir. 1995) and *see MPEP* § 2144.08.

Kaneko et al. Teaches Away, and Therefore is not Combinable

Further, it is impermissible within the framework of 35 U.S.C. §103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one skilled in the art.[12] Further in this regard, As the Court of Customs and Patent Appeals, predecessor to the Federal Circuit, has held:

> All relevant teachings of cited references must be considered in determining what they fairly teach to one having ordinary skill in the art. The relevant portions of a reference include not only those teachings which would suggest particular aspects of an invention to one having ordinary skill in the art, but also those teachings which would lead such a person away from the claimed invention.[13]

The rejections in the Official Action amount, in substance, to nothing more than hindsight reconstruction of Applicants' invention by relying on isolated teachings of the applied art, without considering the overall context within which those teachings are presented. Without benefit of Applicants' disclosure, a person having ordinary skill in the art would not know what portions of [Rostoker et al. and Kaneko et al.] to consider, and what portions to disregard as irrelevant or misleading.[14]

As discussed in the previous Response filed on February 11, 2003, Kaneko et al. is directed to a burn-in and test method of semiconductor wafers and burn-in boards for use in semiconductor burn-in tests which divides each semiconductor wafer into blocks which each include some integrated circuits, and which assigns each block an address to indicate in which part of the semiconductor wafer the integrated circuits of the block are placed.

These addresses in Kaneko et al. are recorded, and detachable carriers also having an identification code are loaded with a block to be tested. As discussed in Kaneko et al. (see col. 5, lines 7-13 when all the burn-in is finished, all carriers are removed from the burn-in board, and

[12] *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.*, 230 USPQ 416 (Fed. Cir. 1986).
[13] *In re Mercier*, 185 USPQ 774, 778 (CCPA 1975).
[14] *In re Wesslau*, 147 USPQ 391, 393 (CCPA 1965).

PAGE 12/14 * RCVD AT 1/9/2004 7:44:31 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:202 293 6229 * DURATION (mm-ss):03-54

then, these carriers are fitted in the IC sockets of an IC tester for testing their characteristics. By handling and loading plural dies in block units, electrical connections to the burn-in and test apparatus are not as complicated, and the procedure is not a laborious as with so-called "die-by-die" loading.

Analysis of burn-in test results in Kaneko et al. permits the locating of defective integrated circuits in semiconductor wafers using the recorded addresses of the blocks, and the identification codes of the carriers. ***Once "good" chips are identified, they are removed from the carrier, and subsequently reattached to an operational carrier.***

That is, Kaneko et al. clearly teaches away from one aspect of the invention, by teaching that, after "good" chips are identified, they are removed from the carrier used in the burn-in test, and subsequently fitted into the IC sockets of an IC characteristics tester. Applicant presumes that subsequent removal from the IC tester and attachment to an end-use carrier follows a successful test of the IC characteristics.

Kaneko et al., therefore, represents a conventional, expensive and time-consuming temporary chip attachment, which is specifically disfavored by the approach of the present application, and which ***teaches away*** from at least one aspect of the invention claimed in independent claim 1.

Kaneko et al. represents an approach which is directly contrary to Applicants' recited limitation by not having ***interconnect wiring sufficient for both operational testing and packaging of the semiconductor devices.*** Kaneko et al. is therefore not properly combinable with Rostoker et al., even if relied upon for teaching limitations asserted by the Examiner to be unrelated to interconnect wiring or use both in operational testing and packaging of semiconductor devices.

Accordingly, reconsideration and allowance of claims 13-29 are requested.

PAGE 13/14 * RCVD AT 1/9/2004 7:44:31 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:202 293 6229 * DURATION (mm-ss):03-54

Application No.: 09/588,617 Docket No.: 21806-00083-US

Allowable Subject Matter

Applicants note with appreciation the indication of allowable subject matter in dependent claims 6-12, but respectfully suggest that amendment of these claims into independent form is not necessary, in light of the allowability of independent claim 1, from which claims 6-12 depend.

Conclusion

In view of the above, each of the presently pending claims 1-32 in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If the Examiner believes that an interview would serve to resolve any remaining issues in this application, the undersigned attorney is available at the telephone number indicated.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 09-0456, under Order No. 21806-00083-US from which the undersigned is authorized to draw.

Respectfully submitted,

By Larry J Hume

Larry J. Hume
Registration No.: 44,163
CONNOLLY BOVE LODGE & HUTZ LLP
1990 M Street, N.W., Suite 800
Washington, DC 20036-3425
(202) 331-7111
(202) 293-6229 (Fax)
Attorney for Applicant

PAGE 14/14 * RCVD AT 1/9/2004 7:44:31 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:202 293 6229 * DURATION (mm-ss):03-54 P.14